PROGRAMMABLE I/O STRUCTURE FOR FPGAs AND THE LIKE HAVING REDUCED PAD CAPACITANCE

ABSTRACT

A programmable device such as a field-programmable gate array (FPGA) has programmable I/O circuitry. In one embodiment, a programmable I/O circuit (PIC) associated with at least first and second pads of the device has an output buffer that is selectively connected to the first and second pads via corresponding first and second transmission gates. The transmission gates enable an outgoing signal from the output buffer to be individually and selectively presented at the pads, while reducing the capacitive loading at each pad when the corresponding transmission gate is open (i.e., when the outgoing signal is not to be presented at that pad).